Amendments to Claims

This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. - 16. (Canceled)

17. (Currently Amended) A method including

coupling each one of a sequence of inputs to a sequence of memories, said sequence of memories having a last memory and a next memory corresponding to each said memory, other than said last memory, wherein each said memory is responsive to a distinct portion of ~~said~~ information supplied to one of said inputs, and wherein at least some inputs have their information applied to all said memories at least once, and to at least some of said memories at least twice;

coupling a result from each said memory, other than said last memory, to its corresponding said next memory in said sequence of memories; and

providing an output of at least one of said memories;

whereby said sequence of inputs is each coupled to said sequence of memories in a pipelined manner to provide said output at a rate substantially equaling one output as each input is received.

18. (Currently Amended) A method as in claim 17, including ~~substantially concurrently~~ providing results ~~responsive to~~ associated with a plurality of said inputs by accessing different sub-sequences of said memories in parallel.

19. (Canceled)

20. (Original) A method as in claim 17, wherein each said input has substantially equal amounts of said information.

21. (Currently Amended) A method as in claim 17, wherein said sequence of inputs includes at least one of: a destination IP address, an IP address, and packet header information.

22. (Currently Amended) A method as in claim 17, wherein said sequence of memories are ~~substantially~~ included in a single monolithic integrated circuit.

23. (Original) A method as in claim 17, wherein said output is responsive to a sequence of individual memory accesses, each said individual memory access being performed at one of said memories.

24. (Canceled)

25. (Original) A method as in claim 23, wherein said sequence of individual memory accesses includes one said individual memory access at each said memory.

26. (Original) A method as in claim 23, wherein said sequence of individual memory accesses includes one said individual memory access at each said memory, followed by a second individual memory access at each said memory for at least a subsequence of said memories.

27. (Original) A method as in claim 23, wherein said sequence of individual memory accesses includes one said individual memory access at each said memory for only a subsequence of said memories.

28. (Original) A method as in claim 17, wherein said sequence of memories collectively include lookup results including at least one datum responsive to each one of said inputs.

29. (Original) A method as in claim 28, wherein said lookup results collectively include a set of packet forwarding information.

30. - 37. (Canceled)

38. (Currently Amended) Apparatus including

a sequence of memories, said sequence having a last memory and a next memory corresponding to each said memory other than said last memory, each said memory being coupled to a distinct portion of one of a sequence of lookup search keys;

each said memory, other than said last memory, being coupled to its corresponding said next memory in said sequence; and

whereby ~~said~~ each input in a sequence of inputs is ~~each~~ coupled to said sequence of memories in a pipelined manner to provide ~~said~~ an output at a rate substantially equaling one output as each input is received.

39. (Currently Amended) Apparatus as in claim 38, wherein a plurality of output registers associated with different memories are each coupled to an output for said ~~circuit~~ apparatus.

40. (Currently Amended) Apparatus as in claim 38, wherein an output register associated with a memory other than said last memory is coupled to a~~n~~ corresponding output ~~for said circuit~~ distinct from said output for the apparatus.

41. (Original) Apparatus as in claim 38, wherein said last memory is coupled to an associated earlier memory in said sequence.

42. (Currently Amended) Apparatus as in claim 38, wherein said sequence of lookup search keys includes at least one of: a destination IP address, an IP address, and packet header information.

43. (Original) Apparatus as in claim 38, wherein said sequence of memories collectively include lookup results including at least one datum responsive to each one of said lookup search keys.

44. (Original) Apparatus as in claim 43, wherein said lookup results collectively include a set of packet forwarding information.